WAFER-LEVEL MOAT STRUCTURES

RELATED APPLICATION

This application is related to application having Serial No. ~~xxx/xxx,xxx~~ 10/672,201 entitled FORMING PARTIAL DEPTH STRUCTURES IN POLYMER FILM, filed on even date with this application, assigned to the same assignee as the assignee of this application, which is hereby fully incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to wafer-level chip scale packages, and more particularly to forming a moat-like structure in a semiconductor wafer to restrict flow of a liquid prior to solidification of the liquid.

2. Description of the Related Art

A wafer-level chip scale package (CSP) is a package for an integrated circuit that is substantially the size of the integrated circuit or of a flip chip, which uses a wafer-level processing technique. Unlike a flip chip, the wafer-level CSP has one or more passivation layers on the active side of the die. Each passivation layer typically comprises a layer of photo-imageable polymer film. The wafer-level CSP is smaller than a standard ball grid array (BGA), typically uses metal traces of a re-distribution layer (RDL) to route solder ball pads to standard pitches, and uses CSP-size solder balls on the re-routed pads. A wafer-level CSP uses a standard surface mount technology assembly process that is also used for BGAs, and does not require underfill.

The use of a polymer collar around a solder ball, or solder bump, to support the solder ball in a wafer-level CSP is well known. When a semiconductor wafer, or wafer, is heated to the reflow temperature of the solder ball, some of the polymer collar material, which is very viscous